CLAIMS

1. A circuit for applying power to mixed mode integrated circuits in a predefined sequence to a first circuit powered by a first voltage and a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit comprising:

a modified IO cell of the second circuit having a driver transistor including a back gate terminal, a gate terminal that is driven by the second circuit, a source terminal that is coupled to a first circuit signal, a drain terminal that is coupled to the second power supply;

a controller circuit coupled to the first voltage and the second voltage supplied as controller circuit inputs and having a plurality of controller circuit outputs; and

a back gate bias application circuit having a plurality of inputs coupled to the plurality of controller circuit outputs, and an output coupled to the backgate of the driver transistor backgate terminal.

2. A circuit for applying power to mixed mode integrated circuits in a predefined sequence to a first circuit powered by a first voltage and a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit comprising:

a modified IO cell of the second circuit having a driver transistor including a back gate connection coupled to the first voltage, a gate terminal that is driven by the second circuit, a source terminal that is coupled to a first circuit signal, and a drain terminal that is coupled to the second power supply;

a controller circuit coupled to the first voltage and the second voltage supplied as controller circuit inputs and having a plurality of controller circuit outputs; and

a back gate bias application circuit having a plurality of inputs coupled to the plurality of controller circuit outputs, and an output coupled to the backgate of the driver transistor backgate terminal.

3. A circuit for applying power to mixed mode integrated circuits in a predefined sequence comprising:

a first circuit powered by a first voltage;

a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit;

an IO cell disposed in the second circuit comprising a driver transistor having a back gate connection coupled to the first voltage, a gate terminal that is driven by the second circuit, a source terminal that is coupled to the first circuit signal, and a drain terminal that is coupled to the second power supply;

a controller circuit coupled to the first voltage and the second voltage supplied as controller circuit inputs and having a plurality of controller circuit outputs; and

a back gate bias application circuit having a plurality of inputs coupled to the plurality of controller circuit outputs, and an output coupled to the backgate of the driver transistor backgate terminal.

4. The circuit for applying power to a mixed mode integrated circuit of claim 3 wherein;

the first circuit is disposed on a first substrate; and

the second circuit is disposed on a second substrate.

5. The circuit for applying power to a mixed mode integrated circuit of claim 3 wherein;

the first circuit is disposed on a substrate; and

the second circuit is disposed on the substrate.

6. The circuit for applying power to a mixed mode integrated circuit of claim 3 wherein;

the first circuit is disposed on a substrate utilizing a 0.30 micron gate length CMOS process; and

the second circuit is disposed on the substrate utilizing a 0.30 micron gate length CMOS process.

7. A circuit for applying power to mixed mode integrated circuits in a predefined sequence comprising:

a first circuit powered by a first voltage;

a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit;

a modified IO cell of the second circuit having a driver transistor including a back gate, a gate terminal that is driven by the second circuit, a source terminal that is coupled to a first circuit signal, a drain terminal that is coupled to the second power supply, a first clamping transistor having a backgate and a source coupled to the backgate of the driver transistor, a drain coupled to the second voltage, and a first clamping transistor gate terminal, a second clamping transistor having a backgate and a source coupled to the backgate of the driver transistor, a drain coupled to the second voltage, and a second clamping transistor gate terminal;

a controller circuit coupled to the first voltage, the second voltage and ground;

a first divider network disposed between the first voltage and the ground and having a first divider tap point that produces a first divider reference voltage;

a second divider network disposed between the second voltage and the ground and having a second divider tap point that produces a second divider reference voltage;

a comparator having a first input coupled to the first divider tap point and having a second input coupled to the second divider tap point, and having a comparator output; and

a bias generator having a bias generator input coupled to the comparator output and a first bias generator output coupled to the first clamping transistor gate, and a second bias generator output coupled to the second clamping transistor gate.

8. A circuit for applying power to mixed mode integrated circuits in a predefined sequence comprising:

a first circuit powered by a first voltage;

a second circuit powered by a second voltage that is less than the first voltage and having the second voltage coupled to the first circuit;

a modified IO cell of the second circuit having a driver transistor including a back gate, a gate terminal that is driven by the second circuit, a source terminal that is coupled to a first circuit signal, a drain terminal that is coupled to the second power supply, a first clamping transistor having a backgate and a source coupled to the backgate of the driver transistor, a drain coupled to the second voltage, and a first clamping transistor gate terminal, a second clamping transistor having a backgate and a source coupled to the backgate of the driver transistor, a drain coupled to the second voltage, and a second clamping transistor gate terminal;

a controller circuit coupled to the first voltage, the second voltage and ground;

a resistive divider disposed between the first voltage and the ground and having a first tap point that produces a first reference voltage that is less than the first voltage;

a divider network coupled to the second voltage including a current source having a first terminal coupled to the second voltage and a second terminal outputting a current, a chain of diodes including a plurality of diodes having each diode of the plurality of diodes coupled such that a positive terminal of a first diode to a negative terminal of a next diode in the chain and having a first positive terminal of the chain coupled to the second terminal of the current source and a last negative terminal of the chain coupled to ground, a node connecting the current source and the chain of diodes forming a second tap point that produces a second reference voltage;

a comparator having a first input coupled to the first tap point and having a second input coupled to the second tap point, and having a comparator output; and

a bias generator having a bias generator input coupled to the comparator output and a first bias generator output coupled to the first clamping transistor gate, and a second bias generator output coupled to the second clamping transistor gate.

9. A method of applying power to mixed mode integrated circuits comprising:

creating a first threshold voltage based upon a first power supply state;

creating a second threshold voltage based upon a second power supply state;

comparing the first threshold voltage to the second threshold voltage;

generating a first bias signal based on the comparison of the first threshold voltage to the second threshold voltage; and

generating a second bias signal based on the comparison of the first threshold voltage to the second threshold voltage.